REMARKS

Claims 12-21 remain active in this application. Claims 1-11 and 22 have previously been canceled. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claim 12 has been amended to emphasize novel features of the invention already represented in the claims. Support for the amendment of the claim is found throughout the application, particularly in Figures 4, 10, and 17 and the description thereof on page 4, lines 23+. No new matter has been introduced into the application.

The Examiner rejects claims 12-14, and 17-21 under 35 U.S.C. 102(b) as being anticipated by Nowak et al.; claims 12-14, 17, 19-21 under 35 U.S.C. 102(b) as being anticipated by Long et al.; claims 15 and 16 under 35 U.S.C. 103(a) referencing Nowak et al. and Lee; claims 15-16, and 18 under 35 U.S.C. 103(a) referencing Long et al. with Lee; and claims 20-21 under 35 U.S.C. 103(a) referencing Nowak et al. or Long et al. with Chau et al. as detailed below. All of these rejections, based on the actual nature of the present invention (as emphasized in the amendment of claim 12), are respectfully traversed.

CLAIMS 12-14, and 17-21: 35 U.S.C. 102(b)
Nowak et al.

The Examiner asserts that claims 12-14, and 17-21 of the present invention are unpatentable over Nowak et al. under 35 U.S.C. 102(b) The Examiner asserts that Nowak et al. teaches an asymmetric field effect transistor comprising: a semiconductor layer 7 formed on an insulator layer 2, wherein the semiconductor layer 7 including impurities supplied thereto and adjacent source and drain regions 39, 41 (Figs. 1D-1G), wherein the impurities in regions 21, 31, 24, 23 have a

location precisely defined by edges of the *gate structure 15* having an oxide layer 17, and located in portions of the semiconductor layer, at the edges of a trench formed by the dielectric layer 35; and a gate structure 15 formed on a portion of the semiconductor layer in the trench formed by the dielectric layer 35 with asymmetrical diode properties at the source and drain regions 39, 41, wherein floating body effect of the transistor is reduced due to the electrical connection between the source and the floating body (col. 1, lines 15-20; col.3, lines 20-26, lines 45-50). The Examiner thus admits that Nowak et al. locates impurities using a gate structure rather than a trench but dismisses this difference as resulting in the same structure as that of Nowak under a product-by-process analysis.

However, Nowak et al. additionally teaches an additional connection formed by "damaged area 23" between the segment of the semiconductor layer between the source and drain regions and either a source or drain region (23 in Figures 1D-1G, col. 3, lines 23-25 and 46-50) of the field effect transistor. This connection is an expedient acknowledged in the specification and noted to present problems to which the invention is directed. The addition of this feature is specifically to avoid a voltage build up in the above-mentioned section of the semiconductor layer (e.g. floating body effects), at the expense of more steps and a more complex and critical manufacturing processes, while proving to be only of questionable effectiveness as noted at page 4, lines 23-32 of the present specification. In Nowak et al. such a structure appears to also involve substantial process criticality and may be difficult to form reliably. Further, this connection requires the accommodation of additional chip space and therefore precludes achievement of the potential integration density that

would otherwise be possible as noted in the above-cited passage of the present disclosure. Thus, Nowak et al. teaches little more of relevance to the present invention than the admitted prior art.

The invention, instead of using an *additional* connection structure as taught in Nowak et al., provides a structure that allows the diodes to be accurately and independently tailored and fabricated (as emphasized by the current amendment to claim 12). The source and drain diode junctions that are manufactured provide additional functional characteristics (e.g. the source or drain diode is leaky to avoid voltage build up in the section of the semiconductor layer between the source and drain regions) without additional components or manufacturing processes. As a result, the number of functional regions, dimensions, and manufacturing complexity of the current invention can be reduced.

As alluded to above, not only the processes used by Nowak et al. differ from those proposed by the applicant, but the two processes do, in fact, result in structurally and electronically different products. For this reason, the Examiner's assertion that claims 12-14, and 17-21 are anticipated under a "product-by-process" analysis is incorrect. Rejection of these claims is therefore respectfully traversed.

Further, it is respectfully submitted that, while recitation of the *structure* for locating the impurities may or may not be properly construed as a "process" recitation, the claims as rejected or, especially amended as requested, contain substantial structural recitations which the Examiner does not demonstrate to be answered by Nowak et al. For example, while the extension implants of Nowak et al. appear to have different shapes, it is not clear that they provide significantly different *"asymmetrical diode properties"*, particularly in view of the evident

requirement in Nowak et al. to provide an additional connection 23 to discharge the otherwise "floating body." For these reasons, the Examiner's rejection of claims 12-14, and 17-21 is respectfully traversed since no *prima facie* demonstration of anticipation has been made even under a product-by-process analysis.

CLAIMS 12-14, 17, 19-21: 35 U.S.C. 102(b)
Long et al.

Similarly, the Examiner asserts that claims 12-14, 17, and 19-21 of the current invention are unpatentable over Long et al. under to 35 U.S.C. 102(b) due to Long et al. teaching an asymmetric field effect transistor comprising: a semiconductor layer (e.g. 14 in Figure 2, col. 4, line 45 through col. 5; or 114 in Figures 8-11; col. 6, line 54 through col. 8)formed on an insulator layer 16 (Figure 2), wherein the semiconductor layer including impurities supplied thereto and adjacent source and drain regions 20, 22, wherein the impurities have a location precisely defined at edges of the *gate structure 48*, located in portions of the semiconductor layer, and located at edges of the *gate structure*, in portions of the semiconductor layer, and at the edges of a trench formed by the dielectric layer 70, 72; and a gate structure 48 formed on a portion of the semiconductor layer with asymmetrical diode properties at the source and drain regions 20,22 (Figure 2; col. 1, lines 60-65), wherein the transistor is formed to avoid floating body effects (col.1, lines 10-13), wherein the floating body effect is substantially avoided and reduced due to the electrical coupling between the source and the floating body (col. 1, lines 1-13, 40-50). Again, the difference in the structure used to locate impurities is admitted but dismissed under a product-by-process analysis. However, the lack of decoupling of implants is particularly evident from

the resulting shapes of the source and drain regions and extension implants, resulting from a single angled implant which is thus even less likely than the structure of Nowak et al. to provide "*asymmetrical diode characteristics*".

Moreover, Long et al., like Nowak et al., also uses additional processes to form additional regions for the purpose of electrical connections (250 in Figure 3, 256 in Figure 13, col. 8, lines 1-6). The addition of this electrical connection is to avoid a voltage build up in the region of the semiconductor layer located between the source and drain regions and is formed by diffusing metal to form silicide below the implanted region and directly into the floating body. This additional component is made at the expense of more steps and more complex and critical manufacturing processes, while proving to be only of questionable effectiveness. Further, it is not clear whether or not this connection may require the accommodation of additional chip space and therefore precludes achievement of the potential integration density that would otherwise be possible. Nevertheless, it is an additional structure requiring additional process steps and possible criticality avoided by the invention. The invention, instead of using an additional connection structure as taught in Long et al., purposefully makes the source or drain region diode junctions asymmetrically leaky using a trench for locating implants that allows the diodes to be accurately and independently tailored and independently and reliably fabricated (as emphasized by the current amendment to claim 12). The product of the applicant's process is thus significantly different in both structure and function of regions therein from that of Long et al. since it provides additional functional characteristics for structures necessarily present in FET's as a result of the manufacturing processes used that Long et al.

does not, thereby resulting in a different product with different components than Long et al.

As stated above, not only the processes used by Long et al. differ from those proposed by the applicant, but the two processes do, in fact, render different products as results. For this reason, the Examiner's assertion that claims 12-14, 17, and 19-21 are "product-by-process" claims is improper. Rejection of these claims is therefore respectfully traversed. For these reasons, the Examiner's rejection of claims 12-14, 17, and 19-21 is respectfully traversed since no *prima facie* demonstration of anticipation has been made even under a product-by-process analysis.

CLAIMS 15 and 16: 35 U.S.C. 103(a)
Nowak et al. in view of Lee

Further, the Examiner asserts that claims 15 and 16 of the current invention are unpatentable over Nowak et al. with Lee according to 35 U.S.C. 103(a) as Nowak et al. teaches an asymmetric field effect transistor while Lee teaches the deposit of an oxide insulator layer that is planarized to form the planarized oxide insulator layer with the gate structure after forming the source and drain regions. As mentioned in the above discussion of claims 12-14 and 17-21, Nowak et al. does not teach the same product or process as the claimed invention and the deficiencies of Nowak et al. are not mitigated by Lee. Accordingly, the Examiner's assertion that Lee teaches the deposit of an oxide layer, as in claim 15, and the planarization of this oxide, as in claim 16, is noted as prior art, discussed in regard to the Damascene process, and claimed only as an addendum to the novel structure recited in claims 12 and 13 on which claims 15 and 16 depend.

CLAIMS 15, 16, and 18
35 U.S.C. 103(a): Long et al. in view of Lee

Similarly, the Examiner asserts that claims 15 and 16 of the current invention are unpatentable over Long et al. with Lee according to 35 U.S.C. 103(a) as Long et al. teaches an asymmetric field effect transistor while Lee teaches the deposit of an oxide insulator layer that is planarized to form the planarized oxide insulator layer with the gate structure after forming the source and drain regions. As mentioned in the above discussion of claims 12-14, 17, and 19-21, Long et al. does not teach the same product or process as the claimed invention. The Examiner asserts that Lee teaches the deposit of an oxide layer, as in claim 15, and the planarization of this oxide, as in claim 16, is noted as prior art, discussed in regard to the Damascene process, and claimed only as an addendum to the novel embodiment stated in claims 12 and 13 on which claims 15 and 16 depend but does not discuss how Lee supplements Long et al. at the points of defining to answer the claim recitations as noted above in order to make a *prima facie* demonstration of obviousness. Since no such demonstration has been made or can be made, this ground of rejection is also clearly in error.

CLAIMS 20 and 21: 35 U.S.C. 103(a)
Nowak et al. or Long et al. in view of Chau et al.

The Examiner further asserts that claims 20 and 21 of the current invention are unpatentable over either Nowak et al. or Long et al. with Chau et al. according to 35 U.S.C. 103(a) as both Long et al. and Nowak et al. teach an asymmetric field effect transistor formed on a semiconductor substrate and forming a doped region by implantation impurities while Chau et al. is cited

to teach a doped region formed by diffusing impurities from a sidewall of a dopes material. As previously shown in the discussion of claims 12-14 and 17-21, neither Nowak et al. nor Long et al. teach a method or a resulting product that is of the same construction or superior to that of the current invention. Nowak et al. and Long et al. teach configurations and manufacturing methods of greater complexity with higher risk for error. Therefore, despite the teachings of Chau et al., rejections of claims 20 and 21 based on 35 U.S.C. 103(a) are rendered moot as neither Nowak et al. or Long et al. in combination with Chau et al. teach the structure recited in the claims.

In view of the foregoing, all of the rejections set forth by the Examiner are in error as to the claims as rejected and, further, are now clearly moot in view of the amendatory language emphasizing recited novel features of the invention. As the present invention is notably different in product and in process than that of both Nowak et al. and Long et al, the grounds for rejection under 35 U.S.C. 102(b) are unsupported and based on improper product-by-process analysis and no *prima facie* demonstration of anticipation or obviousness been made. Further, the differences of the present invention from the teachings of Nowak et al. or Long et al. in combination with Lee or Chau et al. does not support a rejection under 35 U.S.C. 103(a).

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to International Business Machines Corporation (Fishkill)Deposit Account No. 09-0458.

Respectfully submitted,

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